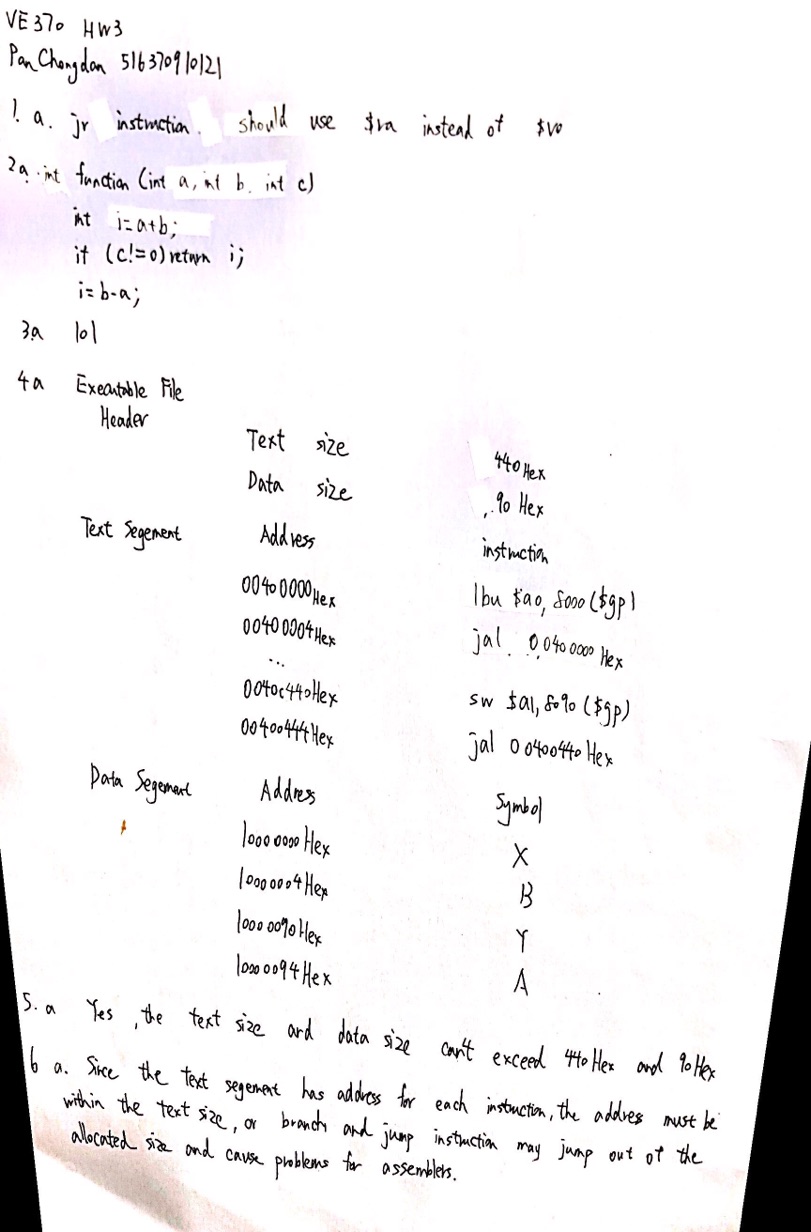
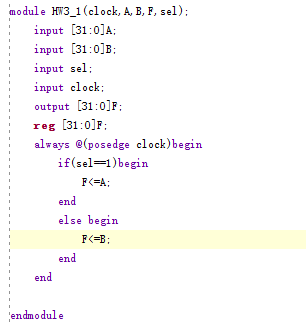
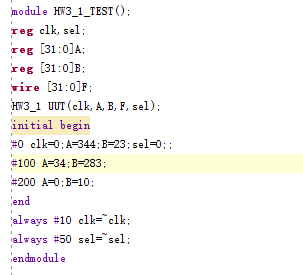
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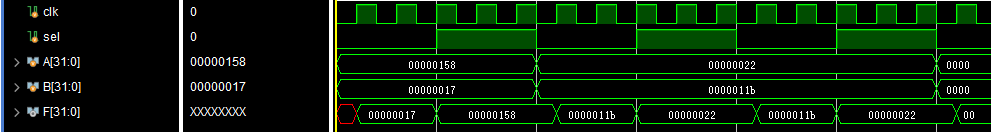
**Problem 7**

**Verilog code**



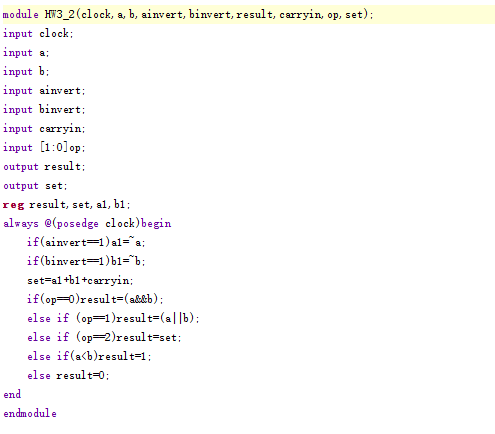
**testbench**



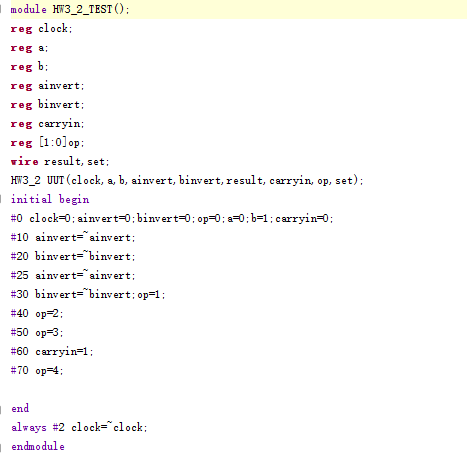


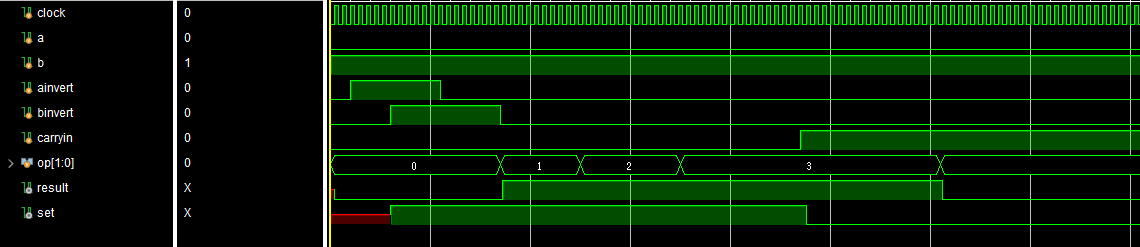
**Problem8**

**Verilog Code**

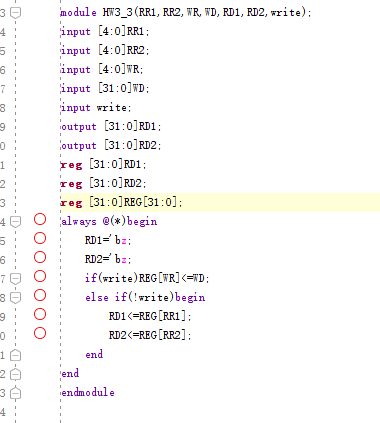


**testbench**

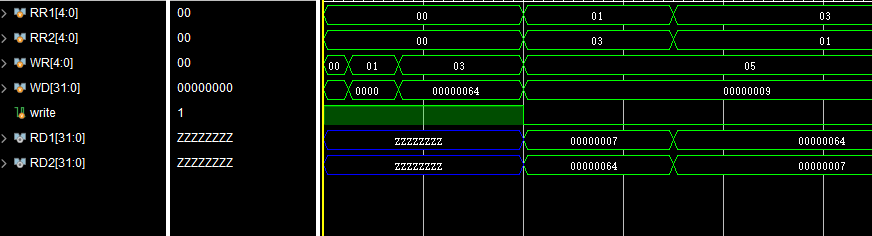




**Problem 9**

**Verilog code**

**testbench**

1